SMH Technologies®

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Driver v. 5.02

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# Interfacing FlashRunner 2.0 with BROADCOM BCM89

SMH Technologies S.r.l.


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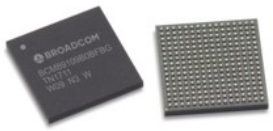
# BROADCOM BCM89 Introduction

Building on Broadcom's extensive BroadR-Reach 100BASE-T1 Ethernet portfolio, Broadcom's Automotive Microcontroller solutions are highly integrated, cost effective, and designed for automotive applications.
These Automotive Ethernet microcontrollers provide a wide range of interfaces to enable customers to design Ethernet based endpoint applications such as cameras, audio amplifiers, graphic displays etc.



**BCM8910x:**

The Broadcom BCM8910x is a fully-integrated BroadR-Reach® camera endpoint microcontroller (MCU) device designed for automotive vision-based applications including rearview and side-view cameras.

The built-in ARM Cortex core supports low latency interrupt processing though the RTOS, runs an Ethernet Audio Video Broadcast (AVB) stack, and processes housekeeping tasks for a wide range of peripherals supporting 100Mbps / 1Gbps Ethernet, GMSL and wireless camera applications.

The device has flexible camera interface that works with many types of camera sensors.
Equipped with a customizable high dynamic range (HDR) imaging pipeline, the BCM8910x allows for scalable camera solutions from low latency video encoders to smart camera MCUs.

A graphics plane overlay with alpha blending allows customers to superimpose guidelines or counters before encoding the video and streaming it over BroadR-Reach Ethernet.

**Features:**

- Integrated BroadR-Reach 100BASE-T1 PHY
- Flexible camera interface allowing customers to interface to a wide range of camera sensors
- Integrated HDR-capable line-based ISP supporting various algorithms in hardware
- On-chip memories for system cost optimization and security
- Low latency video encoder
- Single power supply eliminating the need for expensive external power management circuitry

**Applications:**

- Automotive Rear View Camera
- Automotive Surround View Camera
- Automotive Smart Wired/Wireless Camera
- Automotive Displays



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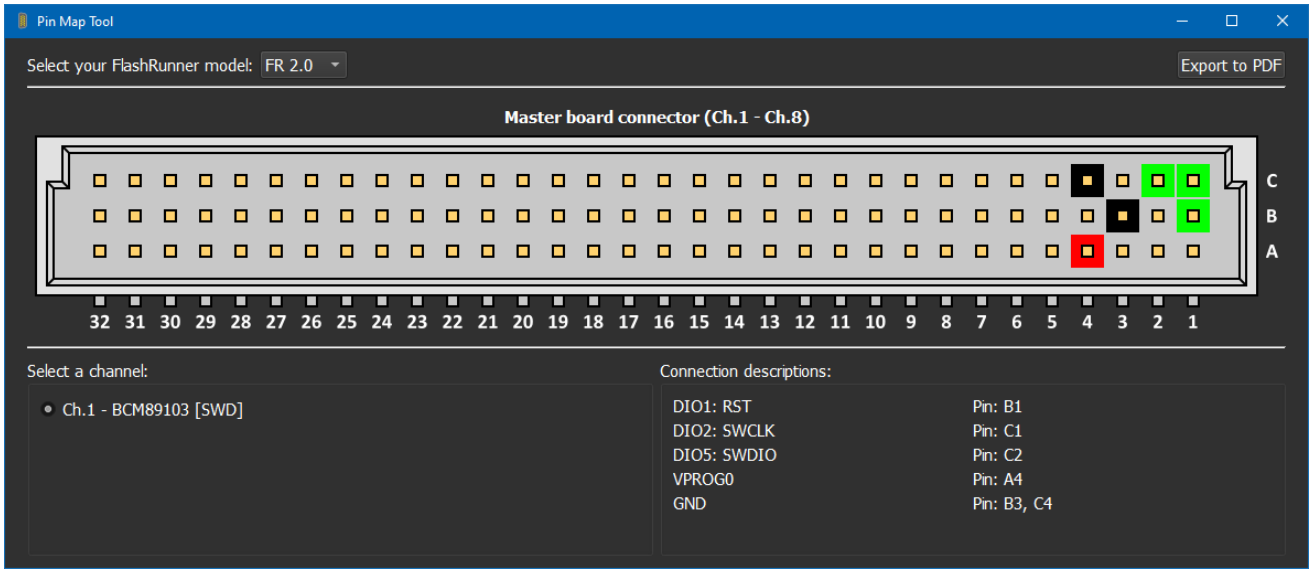
# BROADCOM BCM89 Protocol and PIN map

**BCM89** devices support the SWD protocol.

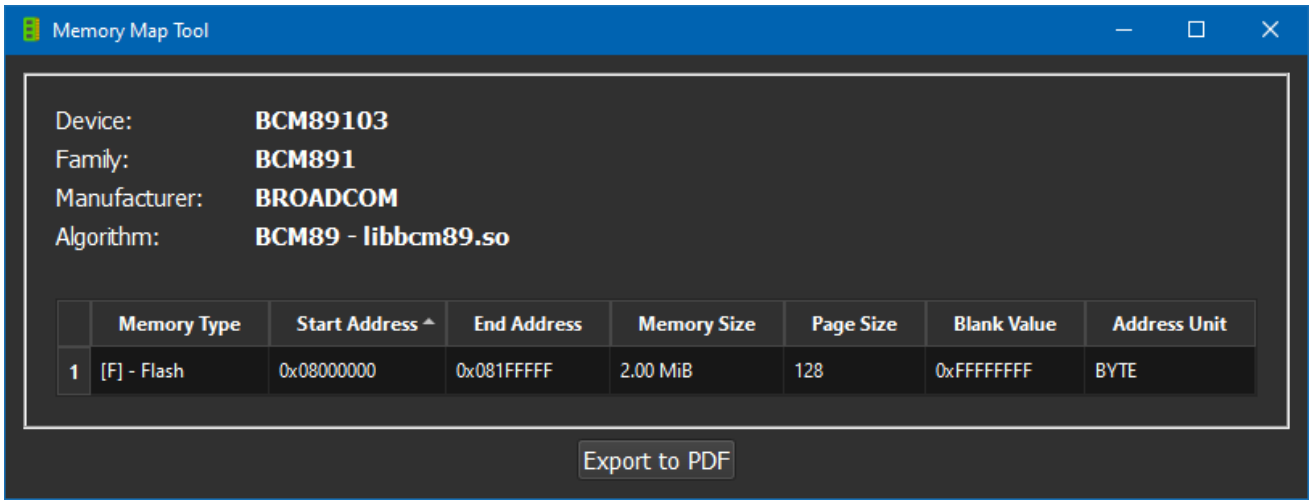
```
#TCSETPAR CMODE <SWD>
```

## BROADCOM BCM89 PIN MAP




## BROADCOM BCM89 Memory Map

| Memory Type | Start Address | End Address | Memory Size | Page Size | Blank Value | Address Unit |
|---|---|---|---|---|---|---|
| [F] - Main Flash | 0x08000000 | 0x081FFFFF | 2.00 MiB | 128 | 0xFFFFFFF | BYTE |





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# BROADCOM BCM89 Driver Parameters

The standard parameters are used to configure some specific options inside BCM89 driver.

## #TCSETPAR ENTRY_CLOCK

*Syntax:* `#TCSETPAR ENTRY_CLOCK <Frequency>`

`<Frequency>` Accepted parameters 4000000, 2000000, 1000000, 500000, 100000 Hz

*Description:* Set the JTAG/SWD frequency used in the Connect procedure before raising the PLL of the device, if the device PLL is available

*Note:* Default value 4.00 MHz

## #TCSETPAR SAMPLING_POINT

*Syntax:* `#TCSETPAR SAMPLING_POINT <Value>`

`<Value>` Accepted values are in the range 1-15

*Description:* Use this parameter to permanently set the sampling point of the FPGA
It is recommended to leave this parameter with the default value

*Note:* Default value 17

# BROADCOM BCM89 Driver Commands

Here you can find the complete list of all available commands for BCM89 driver.

```
F → Main Flash
```

## #TPCMD CONNECT

`#TPCMD CONNECT`

This function performs the entry and is the first command to be executed when starting the communication with the device.

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Trying Hot Plug connect procedure.
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
AP[1] IDR: 0x84770001, Type: AMBA AHB3 bus.
AP[0] ROM table base address 0xE00FD000.
CPUID: 0x411FC271.
Implementer Code: 0x41 - [ARM].
Found Cortex M7 revision r1p1.
Cortex M7 Core halted [0.002 s].
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 4 [Range 3-6].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Time for Connect: 0.116 s.
>|
```



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## #TPCMD MASSERASE

`#TPCMD MASSERASE <F>`
Masserase is available for Flash memory.
This function performs a masserase for all Flash memory.

## #TPCMD BLANKCHECK

`#TPCMD BLANKCHECK <F >`
Blankcheck is available for Flash memory.
Verify if all memory is erased.

`#TPCMD BLANKCHECK <F> <start address> <size>`
Blankcheck is available for Flash memory.
Verify if selected part of memory is erased.
Enter the Start Address and Size in hexadecimal format.

## #TPCMD PROGRAM

`#TPCMD PROGRAM <F>`
Program available for Flash memory.
Programs all memory of the selected type based on the data in the FRB file.

`#TPCMD PROGRAM <F> <start address> <size>`
Program available for Flash memory.
Programs selected part of memory of the selected type based on the data in the FRB file.
Enter the Start Address and Size in hexadecimal format.

## #TPCMD VERIFY

`#TPCMD VERIFY <F> <R>`
R: Readout Mode.
Verify Readout available for Flash memory.
Verify all memory of the selected type based on the data in the FRB file.

`#TPCMD VERIFY <F> <R> <start address> <size>`
R: Readout Mode.
Verify Readout available for Flash memory.
Verify selected part of memory of the selected type based on the data in the FRB file.
Enter the Start Address and Size in hexadecimal format.

`#TPCMD VERIFY <F> <S>`
S: Checksum 32 Bit Mode.
Verify Checksum available for Flash memory.
Verify all memory of the selected type based on the data in the FRB file.

`#TPCMD VERIFY <F> <S> <start address> <size>`
S: Checksum 32 Bit Mode.
Verify Checksum available for Flash memory.
Verify selected part of memory based on the data in the FRB file.
Enter the Start Address and Size in hexadecimal format.

## #TPCMD READ

`#TPCMD READ <F>`
`#TPCMD READ <F> <start address> <size>`
Read function for Flash memory.
The result of the read command will be visible into the Terminal.



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## #TPCMD DUMP

```
#TPCMD DUMP <F>
#TPCMD DUMP <F> <start address> <size>
```

Dump command for Flash memory.
The result of the dump command will be stored in the FlashRunner 2.0 internal memory.

## #TPCMD RUN

*Syntax:* `#TPCMD RUN <Time [s]>`

| | |
|---|---|
| <Time [s]> | Time in seconds (i.e., 2 s). This time is an optional parameter. |

*Prerequisites:* none

*Description:* Move the Reset line up and down quickly if no parameter <Time [s]> is inserted.
`#TPCMD RUN <Time [s]>` instead moves the Reset line down, waits for the entered time and then sets the Reset line high.
This command typically can be used to execute the firmware programmed in the device.

## #TPCMD READ_MEM8

*Syntax:* `#TPCMD READ_MEM8 <Address> <Byte Count>`

| | |
|---|---|
| <Address> | Address in HEX format (i.e., 0x52002020) |
| <Byte Count> | Byte count in decimal format (i.e., 8 -> eight bytes) |

*Prerequisites:* none

*Description:* Read memory byte per byte from target BCM89 device

Note: This command is available from driver version **4.04**
This command prints into Terminal and Real Time Log

*Examples:* Correct command execution: 😊

```
---#TPCMD READ_MEM8 0x52002020 8
Read[0x52002020]: 0xF0
Read[0x52002021]: 0xAA
Read[0x52002022]: 0x16
Read[0x52002023]: 0x14
Read[0x52002024]: 0x00
Read[0x52002025]: 0x00
Read[0x52002026]: 0x00
Read[0x52002027]: 0x00
Time for Read Mem: 0.002 s
```

## #TPCMD READ_MEM16

*Syntax:* `#TPCMD READ_MEM16 <Address> <16-bit Word Count>`

| | |
|---|---|
| <Address> | Address in HEX format (i.e., 0x52002020) |
| <16-bit Word Count> | 16-bit Word count in decimal format (i.e., 4 -> four 16-bit words) |

*Prerequisites:* none

*Description:* Read memory 16-bit word per 16-bit word from target BCM89 device

*Note:* This command is available from driver version **4.04**
This command prints into Terminal and Real Time Log



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*Examples:* Correct command execution: 😊

```
---#TPCMD READ_MEM16 0x52002020 4
Read[0x52002020]: 0xAAF0
Read[0x52002022]: 0x1416
Read[0x52002024]: 0x0000
Read[0x52002026]: 0x0000
Time for Read Mem: 0.002 s
```

## #TPCMD READ_MEM32

*Syntax:* `#TPCMD READ_MEM32 <Address> <32-bit Word Count>`

| | |
|---|---|
| <Address> | Address in HEX format (i.e., 0x52002020) |
| <32-bit Word Count> | 32-bit Word count in decimal format (i.e., 2 -> two 32-bit words) |

*Prerequisites:* none

*Description:* Read memory 32-bit word per 32-bit word from target BCM89 device

*Note:* This command is available from driver version **4.04**
This command prints into Terminal and Real Time Log

*Examples:* Correct command execution: 😊

```
---#TPCMD READ_MEM32 0x52002020 2
Read[0x52002020]: 0x1416AAF0
Read[0x52002024]: 0x00000000
Time for Read Mem: 0.002 s
```

## #TPCMD DISCONNECT

`#TPCMD DISCONNECT`

Disconnect function. Power off and exit.



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# BROADCOM BCM89 Driver Examples

Here you can see a complete example of BROADCOM BCM89 projects.

## 1 – BROADCOM BCM89103 2.00 MB example Commands

```
#TCSETPAR ENTRY_CLOCK 4000000
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 3300
#TCSETPAR CMODE SWD
#TPSETSRC 2MB.frb
#TPSTART
#TPCMD CONNECT
#TPCMD MASSERASE F
#TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TPCMD DISCONNECT
#TPEND
```

## 1 – BROADCOM BCM89103 2.00 MB example Real Time Log

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Trying Hot Plug connect procedure.
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
AP[1] IDR: 0x84770001, Type: AMBA AHB3 bus.
AP[0] ROM table base address 0xE00FD000.
CPUID: 0x411FC271.
Implementer Code: 0x41 - [ARM].
Found Cortex M7 revision r1p1.
Cortex M7 Core halted [0.002 s].
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 4 [Range 3-6].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Time for Connect: 0.116 s.
>|
---#TPCMD MASSERASE F
> Initializing BCM QSPI interface.
> BCM clock frequency: 100.00 MHz.
> BCM QSPI major revision: 4.
> BCM QSPI minor revision: 1.
> BCM QSPI frequency: 6.25 MHz.
Time for Masserase F: 1.643 s.
>|
---#TPCMD BLANKCHECK F
Time for Blankcheck F: 0.316 s.
>|
---#TPCMD PROGRAM F
Time for Program F: 6.840 s.
>|
---#TPCMD VERIFY F R
Time for Verify Readout F: 0.928 s.
>|
---#TPCMD VERIFY F S
Time for Verify Checksum 32bit F: 0.317 s.
>|
```



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```
---#TPCMD DISCONNECT
>|
```

## 1 – BROADCOM BCM89103 2.00 MB example Programming Times

| Operation | Timings FlashRunner 2.0 |
|---|---|
| Time for Connect | 0.105 s |
| | |
| Masserase Flash | 1.643 s |
| Blankcheck Flash | 0.316 s |
| Program Flash | 6.840 s |
| Verify Readout Flash | 0.928 s |
| Verify Checksum Flash | 0.317 s |
| | |
| **Cycle Time** | **00:10.204 s** |

## 2 – BROADCOM BCM89106_W25Q64JV 8.00 MB example Commands

```
#TCSETPAR ENTRY_CLOCK 4000000
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 3300
#TCSETPAR CMODE SWD
#TPSETSRC 8MB.frb
#TPSTART
#TPCMD CONNECT
#TPCMD MASSERASE F
#TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD VERIFY F S
#TPCMD DISCONNECT
#TPEND
```

## 2 – BROADCOM BCM89106_W25Q64JV 8.00 MB example Real Time Log

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Trying Hot Plug connect procedure.
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
AP[1] IDR: 0x84770001, Type: AMBA AHB3 bus.
AP[0] ROM table base address 0xE00FD000.
CPUID: 0x411FC271.
Implementer Code: 0x41 - [ARM].
Found Cortex M7 revision r1p1.
Cortex M7 Core halted [0.002 s].
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 4 [Range 3-6].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Time for Connect: 0.116 s.
```



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```
>|
---#TPCMD MASSERASE F
> Initializing BCM QSPI interface.
> BCM clock frequency: 100.00 MHz.
> BCM QSPI major revision: 4.
> BCM QSPI minor revision: 1.
> BCM QSPI frequency: 6.25 MHz.
Time for Masserase F: 14.022 s.
>|
---#TPCMD BLANKCHECK F
Time for Blankcheck F: 1.850 s.
>|
---#TPCMD PROGRAM F
Time for Program F: 25.808 s.
>|
---#TPCMD VERIFY F R
Time for Verify Readout F: 3.205 s.
>|
---#TPCMD VERIFY F S
Time for Verify Checksum 32bit F: 1.709 s.
>|
---#TPCMD DISCONNECT
>|
```

## 2 – BROADCOM BCM89106_W25Q64JV 8.00 MB example Programming Times

| Operation | Timings FlashRunner 2.0 |
|---|---|
| Time for Connect | 0.116 s |
| | |
| Masserase Flash | 14.022 s |
| Blankcheck Flash | 1.850 s |
| Program Flash | 25.808 s |
| Verify Readout Flash | 3.205 s |
| Verify Checksum Flash | 1.709 s |
| | |
| **Cycle Time** | **00:46.975 s** |



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# BROADCOM BCM89 Driver Changelog

**Info about driver versions prior to 4.00**
All driver versions prior to 4.00 are to be considered obsolete, please update your driver to the latest version.

**Info about driver version 4.00 - 23/07/2021**
Supported BCM89103, BCM89106 and BCM89107.

**Info about driver version 4.01 - 12/08/2021**
Upgraded Connect Under Reset Procedure.
Internal upgrade of the algorithm, no change to the operations it performs.

**Info about driver version 4.02 - 30/08/2021**
Connection procedure updated, now BCM89 driver automatically find the best entry sequence.

**Info about driver version 4.03 - 03/11/2021**
Internal update, upgraded management for reset and halt Cortex core procedure.

**Info about driver version 4.04 - 25/01/2022**
Added READ_MEM8, READ_MEM16, READ_MEM32 commands.

**Info about driver version 4.05 - 14/03/2022**
Internal upgrade of the algorithm, no change to the operations it performs.

**Info about driver version 4.06 - 29/03/2022**
Removed internal Watchdog software. By default, this watchdog is disabled after the power on of the device.

**Info about driver version 4.07 - 16/06/2022**
Print current FPGA version loaded into TPSTART command.
Upgraded internal code to align all drivers.

**Info about driver version 5.00 - 28/07/2022**
Added FPGA for new FlashRunner 2.0 models.

**Info about driver version 5.01 - 05/10/2022**
Increased timeouts into Masserase command and fixed connect procedure.

**Info about driver version 5.02 - 02/10/2023**
Internal driver update.


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